

#4/ICs
Dicing
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MSLIN-98-002CCB



December 10, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: | Serial No. 09/972,639 10/09/01 |
| M.S. Lin |
TOP LAYERS OF METAL FOR HIGH
PERFORMANCE IC'S
Grp. Art Unit: 2823

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on December 13, 2001.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

U.S. Patent 5212,403 to Nakanishi et al., "Integrated Circuit Device having an IC Chip Mounted on the Wiring Substrate and having Suitable Mutual Connections Between Internal Circuits", shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

U.S. Patent 5,501,006 to Gehman, Jr. et al., "Method for Connection of Signals to an Integrated Circuit", shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

U.S. Patent 5,055,907 to Jacobs, "Extended Integration Semiconductor Structure with Wiring Layers", discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film multi-layer wiring decal on the support substrate and over the chip.

U.S. Patent 5,106,461 to Wolfson et al., "High-Density, Multi-Level Interconnects, Flex Circuits, and Tape for TAB", teaches a multi-layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

U.S. Patent 5,635,767 to Wenzel et al., "Semiconductor Device having Built-In High Frequency Bypass Capacitor", teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

U.S. Patent 5,686,764 to Fulcher, "Flip Chip Package with Reduced Number of Package Layers", shows a flip chip substrate that reduces RC delay by separating the power and I/O traces.

Sincerely,



Stephen B. Ackerman,
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